UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/820,662 | 04/07/2004 | Robert J. Drost | SUN04-0191 | 8022 |

22835 7590 01/03/2006

A. RICHARD PARK, REG. NO. 41241
PARK, VAUGHAN & FLEMING LLP
2820 FIFTH STREET
DAVIS, CA 95616

| EXAMINER | |
|---|---|
| SHANKLE, ALEXANDER | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2891 | |

DATE MAILED: 01/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/820,662 | DROST ET AL. |
| | Examiner | Art Unit |
| | Alexander Shankle | 2891 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-7-04 and 8-22-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections – Statutory Double Patenting*

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claims 2 and 16 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1 and 9 of prior U.S. Patent No. 6,925,411. This is a double patenting rejection. Dependent claims 2 and 16, when considered in combination with the limitations of independent claims 1 and 15, respectively, are substantively the same as claims 1 and 9 of prior U.S. Patent No. 6,925,411.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-7, 9-15, 17-21 and 23-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Knight '838.

a. Regarding claims 1 and 15, Knight discloses an apparatus and method for measuring alignment between a first semiconductor die and a second semiconductor die (Fig.11A-11B and Col.28 Lines 9-28), comprising: applying a pattern of voltage signals to a two-dimensional array of conductive transmitter elements that form a transmitter array on the first semiconductor die; wherein the transmitter array on the first semiconductor die is located over a corresponding two-dimensional array of conductive receiver elements that form a receiver array on the second semiconductor die; wherein a voltage signal applied to a transmitter element induces a voltage signal in one or more receiver elements (Col.23 Lines 35-67); amplifying voltage signals induced in receiver elements in the receiver array (Col.24 Lines 3-27); and analyzing the amplified signals to determine an alignment between the first semiconductor die and the second semiconductor die (Col.36 Line 25 to Col.37 Line 8).

b. Regarding claims 3 and 17, Knight discloses the apparatus of claim 15 and the method of claim 1, wherein the transmitter array is organized as a two-dimensional n x m grid including nm conductive elements; and wherein the receiver array includes at least three conductive elements that are not collinear (Fig.23A).

c. Regarding claims 4 and 18, Knight discloses the apparatus of claim 15 and the method of claim 1, wherein the receiver array is organized as a two-dimensional n x m grid including nm conductive elements; and wherein the transmitter array includes at least three conductive elements that are not collinear (Fig.23A).

d. Regarding claims 5 and 19, Knight discloses the apparatus of claim 15 and the method of claim 1, wherein the driving mechanism and the analysis mechanism are configured to determine six degrees of alignment (Col.33 Lines 38-45). Knight does not specifically name six degrees of spatial alignment, but it is inherent that they exist in the determination of proximity alignment of two half-capacitor elements to each other.

e. Regarding claims 6 and 20, Knight discloses the apparatus of claim 19 and the method of claim 5, wherein determining the alignment involves analyzing coupling capacitances between individual receiver elements and individual

transmitter elements to determine their spatial alignment by means of gain circuitry and computerized analysis (Col.33 Line 52 to Col.34 Line 39).

f. Regarding claims 7 and 21, Knight discloses the apparatus of claim 20 and the method of claim 6, wherein the analysis mechanism is configured to determine a nearest neighbor mapping between receiver elements and transmitter elements (Col.33 Line 52 to Col.34 Line 39).

g. Regarding claims 9 and 23, Knight discloses the apparatus of claim 19 and the method of claim 5, wherein the apparatus is configured to determine spatial alignment by summing capacitances between individual receiver elements in the receiver array and all transmitter elements in the transmitter array, thereby effectively considering the transmitter array to be one large plate (Col.15 Lines 43-53).

h. Regarding claims 10 and 24, Knight discloses the apparatus of claim 19 and the method of claim 5, wherein the apparatus is configured to determine spatial alignment by summing capacitances between individual transmitter elements in the transmitter array and all receiver elements in the receiver array, thereby effectively considering the receiver array to be one large plate (Col.15 Lines 43-53).

i. Regarding claims 11 and 25, Knight discloses the apparatus of claim 15 and the method of claim 1, wherein the apparatus is configured to electrically vary the pitch of the transmitter array by grouping together adjacent transmitter elements. Knight does not expressly state, "electrically vary the pitch", but this concept is implied by the flexibility to couple multiple modules to a single module (Fig.39).

j. Regarding claims 12 and 26, Knight discloses the apparatus of claim 15 and the method of claim 1, wherein the apparatus is configured to electrically vary the pitch of the receiver array by grouping together adjacent receiver elements. Knight does not expressly state, "electrically vary the pitch", but this concept is implied by the flexibility to couple multiple modules to a single module (Fig.39).

k. Regarding claims 13 and 27, Knight discloses the apparatus of claim 15 and the method of claim 1, wherein transmitter elements and receiver elements are: rectangular (Fig.23A) and "the size and shape of half-capacitors ... can be advantageously optimized..." (Col.15 Lines 58-62).

l. Regarding claims 14 and 28, Knight discloses the apparatus of claim 15 and the method of claim 1, wherein transmitter elements are located in a metal layer of the first semiconductor die and are not covered by higher layers of metal;

and wherein receiver elements are located in a metal layer of the second semiconductor die and are not covered by higher layers of metal (Fig.1 and Col.15 Lines 36-42).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knight '838 in view of Nabors [1992].

a. Regarding claims 8 and 22, Knight discloses the apparatus of claim 19 and the method of claim 5, wherein the analysis mechanism is configured to determine a spatial alignment of conductive elements (Col.33 Lines 38-45), however, Knight does not specifically teach the use of a mapping function generated by a three-dimensional capacitance field solver simulation.

b. Nabors teaches the use of a 3-D capacitance field solver algorithm to generate a mapping function of capacitance for conductive elements of almost any geometry.

c. At the time of the invention, it would have been obvious to one of ordinary skill in the art to use Nabors' capacitance field solver to determine the spatial alignment of conductive elements in the Knight method and apparatus. The motivation for doing so would have been to provide an efficient way of indicating capacitive coupling fields to the Knight method by decreasing the computational time required to extract a capacitance model while maintaining accuracy as taught by Nabors.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Doyle '400, Lu '679 and Goethem '277 relate to electronic signaling between two devices by capacitive coupling. Mehrotra '508 is an on-chip capacitive field modeling method and apparatus. Miller '071 is drawn to a system of capacitive incremental position measurement and motion control.

**USPTO CONTACT INFORMATION**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, Alex Shankle at (571)272-3476. The examiner can normally be reached on M-F 9am to 6pm. If the examiner is not available, the examiner's supervisor, Bill Baumeister can be reached at (571)272-1722.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander J Shankle

Patent Examiner, Art Unit 2891

8 December 2005

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800